REMARKS

This is in response to the Office Action dated November 17, 2004. Claims 1, 4-5, 7-9, 11 and 24 are pending.

Formality Objections

Claims 1, 7 and 24 stand objected to in paragraph 1 of the Office Action. The Office Action contends that a transistor "cannot be fully on and in a semiconductor simultaneously." However, the claims do not say this. In particular, the claims do not require that a transistor be "*fully*" on and in a semiconductor layer simultaneously. Instead, the claims require that a transistor is formed on and in a semiconductor layer (e.g., the second semiconductor layer 33 in Fig. 3). This is a correct recitation, for example since the S/D regions are "in" the semiconductor layer 33 and the gate 35 is over the semiconductor layer 33 (e.g., see Figs. 1 and 3 of the instant application). Thus, it is respectfully submitted that this objection should be withdrawn.

The other formality issues have been addressed and overcome.

Section 112 Rejections

The Examiner continues to object to the word "simultaneously." While applicant does not agree with this objection, the word "simultaneously" has been removed from the claims rendering this rejection moot. The Examiner on page 3 of the Office Action suggested that this would overcome the Section 112 rejection. Accordingly, it is respectfully requested that the Section 112 rejection be withdrawn.

Moreover, it is pointed out that a transistor being "substantially completely depleted" means that a depletion layer on the gate electrode side and a depletion layer on the semiconductor layer surface side are connected to each other. In the case of an NMOS transistor for example, "substantially completely depleted in the standby state" means that the transistor is

in an OFF state at a gate voltage of 0 V for example and the depletion layers are connected to each other. The transistors being "substantially completely depleted" in the operative state means, in the case of an NMOS transistor for example, that the transistor is in an ON state by application of a given voltage (e.g., positive voltage) and the depletion layers are connected to each other. By making the transistors "substantially completely depleted" in the operative state, the parasitic capacitance can be advantageously reduced thereby permitting a higher speed of operation to be achieved. Furthermore, the transistor may change the threshold voltage depending upon the standby/operative state. In other words, when the transistor is in the standby state, its threshold is changed to prevent (or reduce) a current from flowing in the transistor; that is, to reduce an OFF current. When the transistor is of the NMOS type for example, a bias voltage is applied to the well on the substrate side so that the threshold is increased. When the transistor is in the operative state, its threshold is changed to help a current to easily flow in the transistor; that is, to allow for a high speed operation of the transistor. When the transistor is of the NMOS type, a bias voltage is set so as to lower the threshold.

In this regard, in certain example embodiments where the transistor structure has an NMOS transistor and a PMOS transistor respectively formed in independent wells, a bias voltage can be applied separately to each well. This allows the two transistors to be substantially completely depleted in the standby state. This is supported by the instant specification, for example, at page 24, lines 9-25.

Finally, it is respectfully submitted that the phrase "substantially electrically isolated" is clear and definite. This word "substantially" is used to take into account separation by only the first semiconductor layer of the multilayer SOI substrate. The claims are entirely clear and

definite in that there is general electrical isolation in this respect as will be appreciated by those of skill in the art.

Claim 1 – Art Rejection Under Section 103(a)

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Burr in view of Yamaguchi and/or K '470. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that "a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer, a buried insulating film, and a second semiconductor layer stacked in this order on a support substrate; a first MOS transistor formed on and in the second semiconductor layer of the SOI substrate; . . . . an impurity diffusion layer of the first conductivity type is formed in the first semiconductor layer of the multi-layer SOI substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the first semiconductor layer of the multi-layer SOI substrate, wherein said source and drain regions as well as said channel are all formed in the second semiconductor layer of the multi-layer SOI substrate; . . . . the first MOS transistor comprises a P-type well and the second MOS transistor comprises an N-type well formed in the first semiconductor layer of the multi-layer SOI substrate, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other, and wherein the impurity diffusion layer makes up at least part of the P-type well of the first MOS transistor." The cited art fails to disclose or suggest these aspects of claim 1 for at least the following reasons.

First, claim 1 requires that the impurity diffusion layer and the S/D regions be of *different* conductivity types and be in different semiconductor layers of a multi-layer SOI

substrate, and that the contact hole reaches the impurity diffusion layer so that the different bias voltages are applied to the first semiconductor layer via the impurity diffusion layer, and wherein the conductor in the contact hole is electrically isolated from the second semiconductor layer by at least the device isolation region. The Office Action admits that Burr fails to disclose or suggest these aspects of claim 1, and thus cites to KR '470. The Section 103(a) combination of Burr and KR '470 is fundamentally flawed and legally incorrect.

Burr discloses a diffusion layer (e.g., well 750) and source/drain regions (e.g., 712, 714) of *different* conductivity types. As admitted in the Office Action, Burr does not describe or suggest a potential applied from above via an isolation region which is switched between the standby and operative states as required in claim 1. However, given these different conductivity types, Burr repeatedly states that the diffusion layer must be aligned directly under only the intrinsic channel region (i.e., diffusion layer ***cannot*** extend outside of the S/D regions, and thus cannot receive the contact as claimed here) (e.g., col. 5, lines 54-56; col. 7, lines 18-20). Thus, Burr requires a well contact from the substrate side (not the transistor side) which is directly contrary to the invention of claim 1.

Recognizing that Burr fails to disclose or suggest the diffusion layer contact arrangement required by claim 1, the Office Action cites to KR '470. KR '470 discloses an expanded back gate which extends past the channel and source/drain regions so that a contact can be made from the transistor side of the substrate. KR '470 has an N-well and P-well which contact each other-directly contrary to what claim 1 requires. Moreover, the only reason that KR '470 can extend its back gate 20, 24 past the channel and source/drain regions to enable contact is because the back gate is always of the *same* conductivity type as the source/drain (opposite of Burr). When KR '470 is applied to an n-type MOSFET, both the back gate and source/drain regions are apparently

n-type, and when applied to a p-type MOSFET both the back gate and the source/drain regions are p-type. In KR '470, since the back gate and source/drain regions have the same conductivity type, the back gate can be expanded without adversely affecting transistor operation.

However, there is no suggestion in the art of record that would have caused one of ordinary skill in the art to have expanded a diffusion layer as required by claim 1 so as to be located under at least the channel and source/drain regions in a situation where the diffusion layer is of a *different* conductivity type than the source/drain regions as required by claim 1. In contrast, Burr teaches that this should not be done. KR '470 also teaches directly away from the invention of claim 1 since KR requires that the adjacent P and N wells of adjacent different transistors contact each other. The invention of claim 1, by having the N-well and P-well formed via the substrate, can alleviate contact resistance between the wells and/or increase the parasitic capacitance between the wells, thereby allowing the latch-up resistance to be improved. Accordingly, the Section 103(a) combination of Burr and KR '470 is fundamentally flawed and incorrect.

Second, none of the cited references disclose or suggest the claimed SOI substrate that includes at least a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer, a buried insulating film, and a second semiconductor layer stacked in this order on a support substrate. Furthermore, claim 1 requires that the impurity diffusion layer and the S/D regions be of different conductivity types and be in different semiconductor layers of the multi-layer SOI substrate (e.g., see original claim 12; and pg. 16, lines 13-19 of the instant specification). None of the cited references disclose or suggest these underlined features of claim 1. Thus, even if the references were combined as alleged in the Office Action (which would be incorrect in any event), the invention of claim 1 still would not be met in this regard.

Third, Burr relates to an entirely different type of device than does KR '470. Burr's adjacent transistors 702 and 704 are electrically isolated from one another via "Ox" provided therebetween. Since the overall transistors 702 and 704 are electrically isolated in Burr, it makes sense to also electrically isolate the two wells located beneath the respective transistors. However, in clear contrast with Burr, adjacent transistors in KR '470 are not electrically isolated from one another. Instead, they share the same semiconductor material and the alleged back gates are immediately adjacent. In other words, KR '470 and Burr utilize opposite types of structure. Thus, one of ordinary skill in the art would not have made the alleged combination of opposite types of structure as alleged in the Office Action.

Claim 7

Claim 7 requires that "a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer, a buried insulating film, and a second semiconductor layer stacked in this order on a support substrate; a first MOS transistor formed on and in the second semiconductor layer of the multi-layer SOI, an element isolating region formed in the second semiconductor layer, a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the first semiconductor layer of the multi-layer SOI substrate for the first MOS transistor . . . . the first and second MOS transistors are of different conductivity types on the SOI substrate, and wherein bias voltages applied via said contact portion for the first transistor and a separate contact region including a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted in the standby state; and wherein the first MOS transistor comprises a P-type well and the second MOS transistor comprises a N-type well formed in the first semiconductor layer of the multi-layer SOI

substrate, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other." The cited art fails to disclose or suggest these features of claim 7.

Claim 24

Claim 24 requires "a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer of a first conductivity type, a buried insulating film, and a second semiconductor layer stacked in this order; a PMOS transistor and an NMOS transistor formed on and in the second semiconductor layer of the SOI substrate, a p-type well formed in the first semiconductor layer of the SOI substrate for the NMOS transistor and an n-type well formed in the first semiconductor layer of the SOI substrate for the PMOS transistor, the p-type and n-type wells being substantially isolated from one another; and respective contact portions for applying to the first semiconductor layer of the multi-layer SOI substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are substantially completely depleted in the standby state, wherein said contact portions are electrically insulated from said second semiconductor layer." Again, the cited art fails to disclose or suggest these features of claim 24.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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